

# IMAGINATION UNIVERSITY PROGRAMME



## Essential learning about RISC V

**"RVfpga" provides the foundation knowledge and hands-on experience that the *next generation of Programmers and Engineers need to harness the potential of RISC-V*. Complete materials structured for Teachers, and supported by videos, workshops and online courses.**

Suitable for under graduate classes, self-study, and industry training. Everything a Teacher needs: how to set-up the course, the hardware and software tools, lecture slides, student manuals and supplementary materials. Even suggested exam questions! Comprehensive materials for three semesters.

- Available in seven languages: English, Simplified Chinese, Traditional Chinese, Japanese, Korean, Spanish & Turkish (+ Russian Jan'22).
- 20 Labs with detailed instructions, examples, short questions and practical exercises with solutions, giving teachers flexibility to choose between a practical and an exam-based structure for the course.
- Provided in both .pdf and .pptx/.docx enabling customisation by Teachers to suit their needs.

### **By academics for academics!**

RVfpga is a collaborative effort between Imagination Technologies' University Programme (IUP), leading academics, and supporting companies.

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“RVfpga-SoC: An Introduction to SoC Design” enables users to gain hands-on experience of building a System-on-Chip. RVfpga-SoC guides users through the interconnect options, adding peripherals, then running an RTOS on the SoC. There’s also an exercise to run Tensorflow Lite on the SweRVolf core. The RVfpga system uses Chips Alliance’s SweRVolf SoC, based on Western Digital’s RISC-V SweRV EH1 core. SweRV is a fully-verified production level processor core. It is fully open-source, and is now being used by several companies in silicon, including by Western Digital in data storage and Imagination Technologies in their latest GPUs.

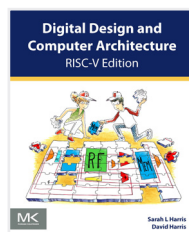
SweRV is at the centre of a vibrant expanding ecosystem with many useful open-source and commercial tools available, including Simulators, Models, Integrated Development Environments, Virtual Hardware and pre-configured FPGA-ready SoC implementations. We believe passionately in sharing real-world in-silicon solutions with Students. Why use a “simplified education core” when you can use industrially proven designs?

#### Software

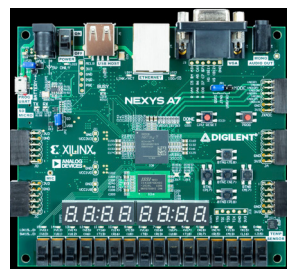
- Xilinx Vivado 2019.2 WebPACK
- Microsoft’s Visual Studio Code
- PlatformIO with Chips Alliance platform, which includes: RISC-V Tool-chain, OpenOCD, Verilator HDL Simulator, WD Whisper ISS

#### Hardware

- Digilent Nexys A7, Nexys A7 -100T or Nexys 4 DDR FPGA Board
- Core: Western Digital’s SweRV EH1
- SoC: Chips Alliance’s SweRVolf



Digital Design & Computer Architecture: RISC-V Edition, by Sarah Harris & David Harris



Digilent: Nexys A7-100T FPGA Board

#### Sponsors and Supporters:



## Semesters 1&2: RVfpga: Understanding Computer Architecture!

Lecture Topic	Details
Lab 0	RVfpga Labs Overview
Lab 1	Creating a Vivado Project
Lab 2	C Programming
Lab 3	RISC-V Assembly Language
Lab 4	Function Calls
Lab 5	Image Processing: Projects with C & Assembly
Lab 6	Introduction to I/O
Lab 7	7-Segment Displays
Lab 8	Timers
Lab 9	Interrupt-Driven I/O
Lab 10	Serial Buses
Lab 11	SweRV EH1 Configuration and Organization. Performance Monitoring
Lab 12	Arithmetic/Logical Instructions: the add instruction
Lab 13	Memory Instructions: the lw and sw instructions
Lab 14	Structural Hazards
Lab 15	Data Hazards
Lab 16	Control Hazards. Branch Instructions: the beq Instruction. The Branch Predictor.
Lab 17	Superscalar Execution
Lab 18	Adding New Features (Instructions, Hardware Counters) to the Core
Lab 19	Memory Hierarchy. The Instruction Cache.
Lab 20	ICCM and DCCM

## Semester 3: RVfpga-SoC: Introduction to SoC Design

Lecture Topic	Details
Lab 1	Introduction to RVfpga-SoC
Lab 2	Running Software on the RVfpga SoC
Lab 3	Introduction to SweRVolf and FuseSoC
Lab 4	Building and Running Zephyr on the SweRVolf
Lab 5	Running Tensorflow Lite on SweRVolf

## Other Teaching Materials from Imagination

Our teaching material packages include presentation slides, an instructor's guide, a student manual, lab exercises, test questions and reference guides, supplied in both PDF and source PowerPoint & Word formats.

### Introduction to Mobile Graphics v2.2 ("2020 Edition")

<b>Scope</b>	The first full semester course on Mobile Graphics, with Lectures and Labs	<b>Tool-Chain</b>	
<b>Audience</b>	3rd year BSc/MSc Gaming and CS Students	<b>Videos</b>	7 modules incl: Architecture, PVR framework, Open GL ES 2.0, Debugging with PVR Trace
<b>Hardware</b>	Chromebook, Android phones / tablets, BeagleBone Black OR: Softwear Emulator	<b>Support</b>	PowerVR Developer's Fourm & IUP Course Fourm
<b>Partners</b>	BeagleBoard.org, University of Hull	<b>Languages</b>	English, Simplified / Traditional Chinese, Japanese, Korean.

### Edge AI – Principles and Practices

Rigorous and complete. A foundation course for under-graduates  
Pilot courses to be released in Q1'22 - apply now

<b>Scope</b>	The course is based on the development of 9 laboratory units, which will cover most of the fundamental algorithms and typical applications in Edge AI, follows a case-study format and fits a typical semester course.	<b>Platform</b>	SEED Studio "Pumpkin" i300 board running Imagination's Neural Compute Software Development Kit
<b>Audience</b>	3rd year BSc EE and CS Students	<b>Authors</b>	Prof. Luis Pinuel Moreno & Prof. Francisco D. Igual - Universidad Complutense de Madrid (Spain). Prof. Xiaohui Duan - Peking University (China)
<b>Languages</b>	English. Simplified and Traditional Chinese to follow.	<b>Support</b>	IUP Forum

### Joining the IUP & Requesting Materials...

#### IUP Website

IUP website: teaching materials, video tutorials, forums, suggested hardware, recommended textbooks, pictures, news, and workshop / event listings.

#### Joining the IUP

1. Register online at <http://university.imgtec.com/register/>
2. Activate your account from the verification email

3. Visit the IUP teaching materials page: <https://university.imgtec.com/teaching-download/>
- Request the materials you want
- Tell us what you plan to do
4. Downloads are usually approved within 48 hours

The IUP homepage:

<https://university.imgtec.com>