**RVfpga Modifications**

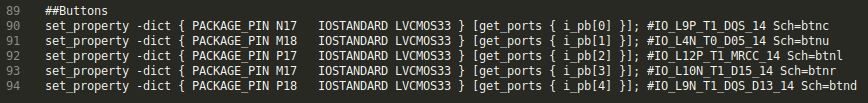
In this document we summarize the changes that you must make to the RVfpga SoC to complete the exercises in RVfpga Labs 6-10. This RVfpga extended version, available at *[RVfpgaPath]/RVfpga/Labs/RVfpgaLabsSolutions/src*, includes all of the changes together. We describe the specific changes necessary for completing each of the lab exercises here.

Exercises that require changes to the RVfpga SoC are:

* Lab 6 – Exercise 2
* Lab 6 – Exercise 3
* Lab 7 – Exercise 3
* Lab 8 – Exercise 2
* Lab 9 – Exercise 2

**Lab 6 – Exercise 2.** Extend RVfpga to access the five on-board pushbuttons.

* rvpfga.xdc



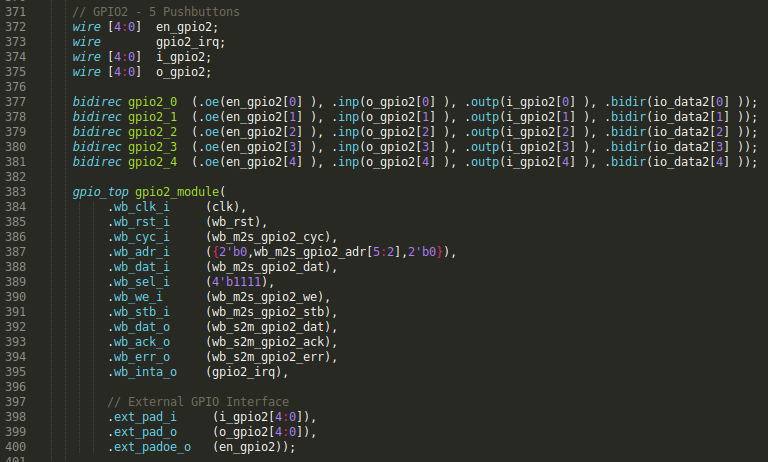
* rvpfga.sv



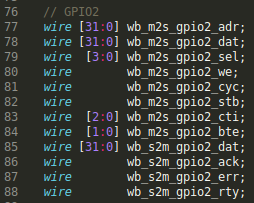


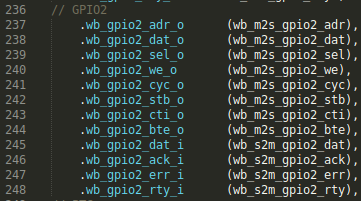
* swervolf\_core.v



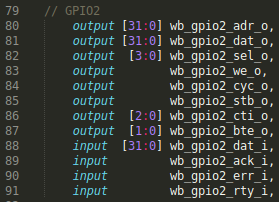


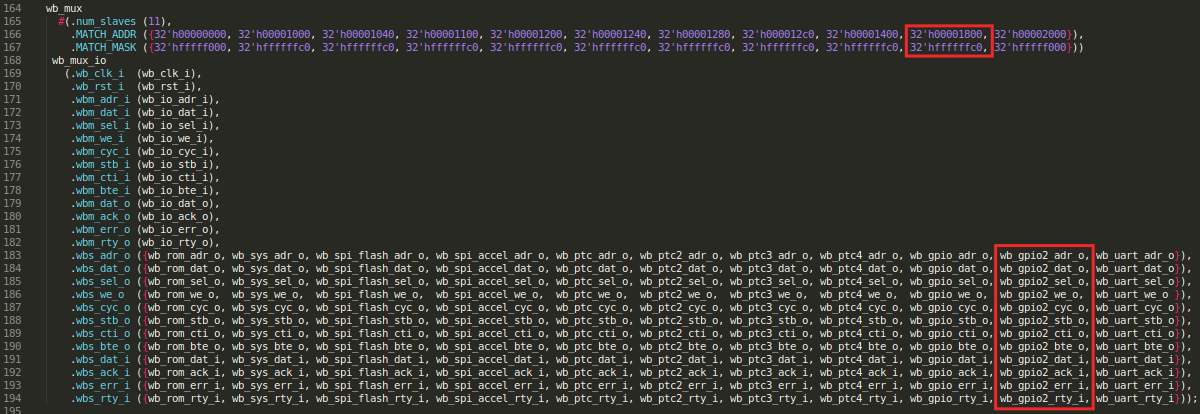
* wb\_intercon.vh





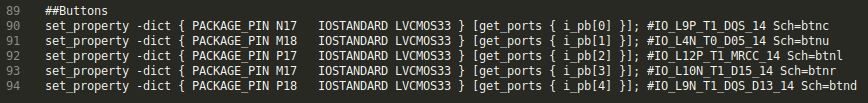
* wb\_intercon.v





**Lab 6 – Exercise 3.** Design another controller in RVfpga for the five on-board pushbuttons. In contrast to the previous exercise, in this case you must implement your own GPIO controller in Verilog/SystemVerilog.

* rvpfga.xdc



* rvpfga.sv





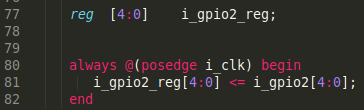
* swervolf\_core.v





* swervolf\_syscon.v

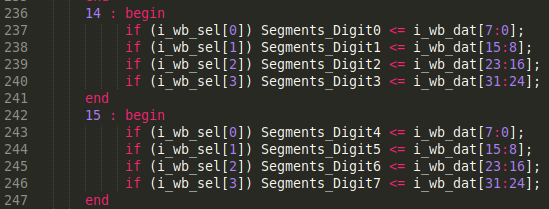


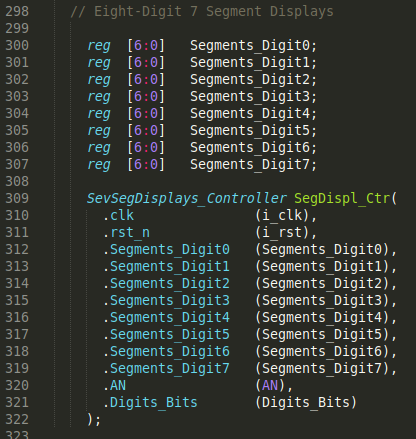


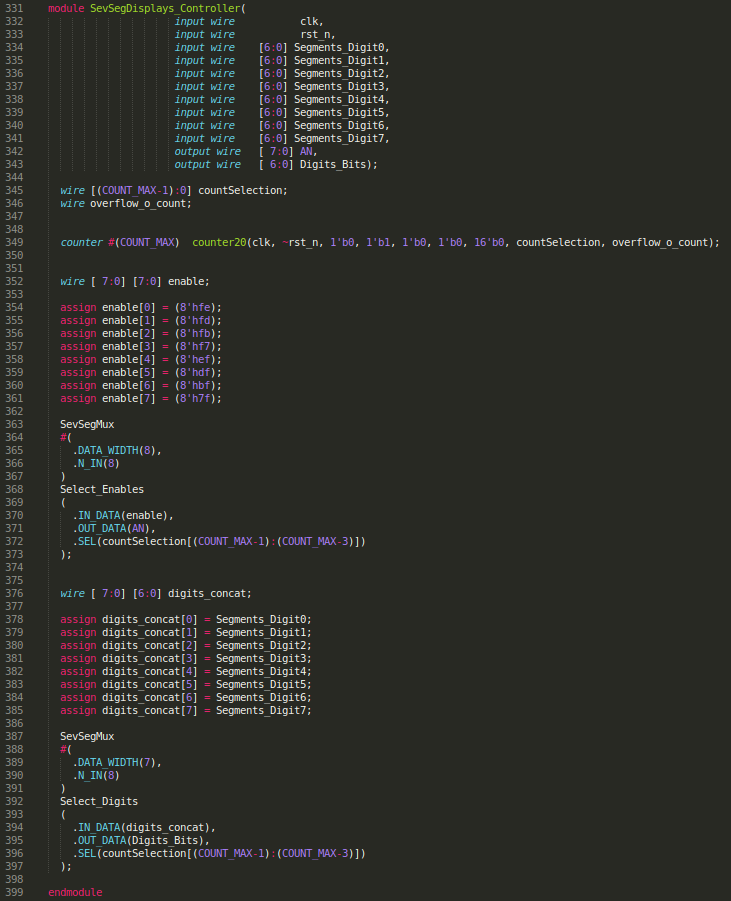


**Lab 7 – Exercise 3.** Modify the controller described in this lab so that the 8-digit 7-segment displays can show any combination of ON/OFF LEDs.

* swervolf\_syscon.v

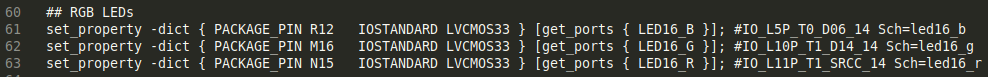




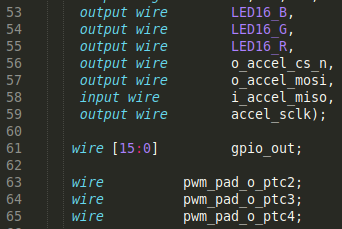


**Lab 8 – Exercise 2.** Modify RVfpga so that it connects the PWM output signal of the timer to one of the two tri-color LEDs available on the Nexys A7 board.

* rvpfga.xdc



* rvpfga.sv

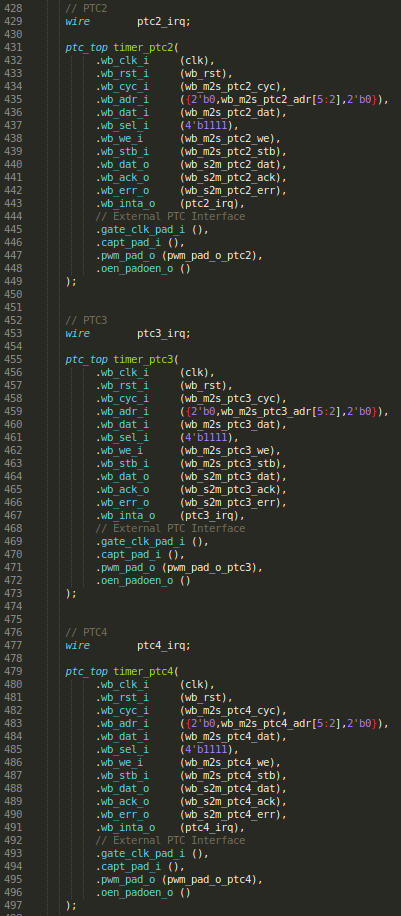




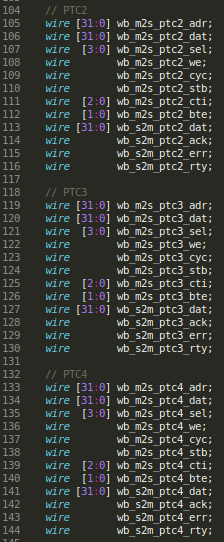


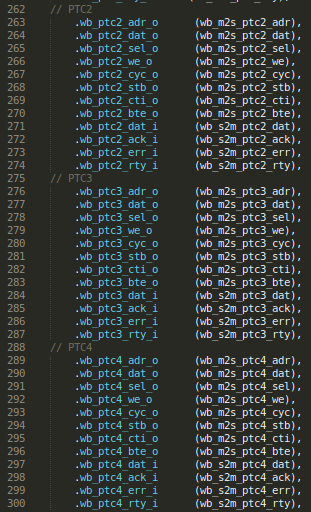
* swervolf\_core.v



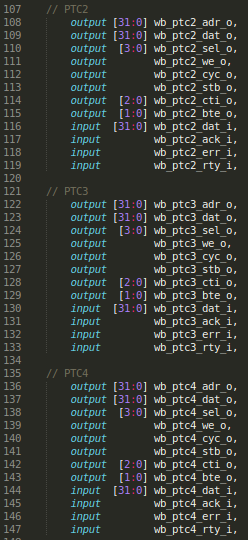


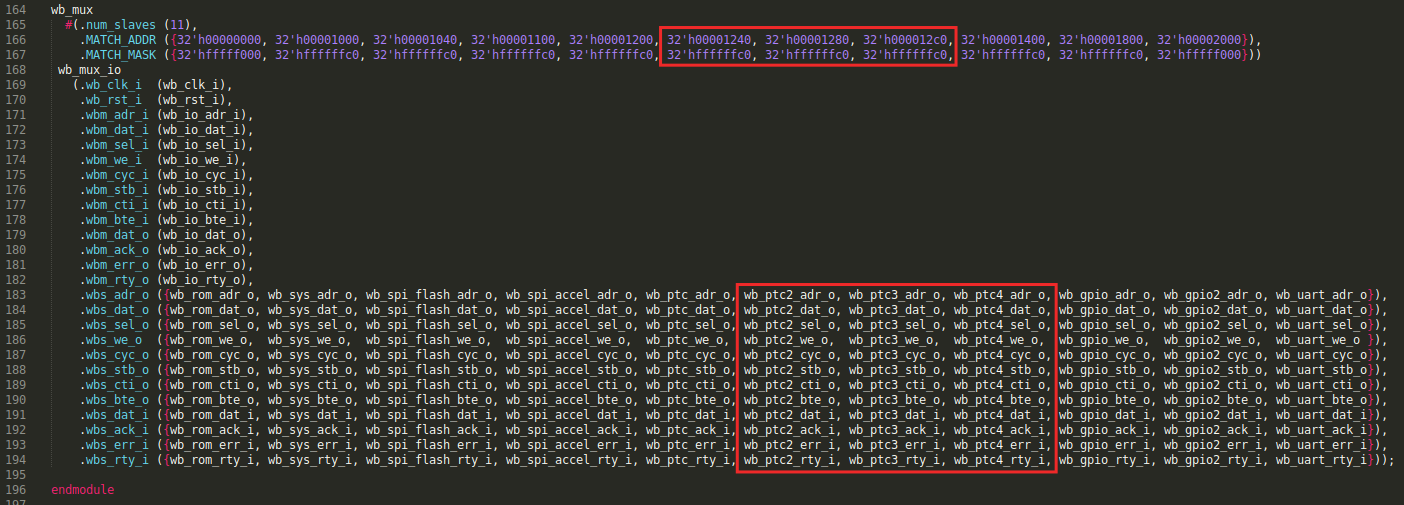
* wb\_intercon.vh





* wb\_intercon.v





**Lab 9 – Exercise 2.** Expand RVfpga so that it includes a second interrupt source through IRQ4 that comes from the second GPIO that you included in Lab 6 for controlling the on-board pushbuttons.

* swervolf\_core.v



* swervolf\_syscon.v



