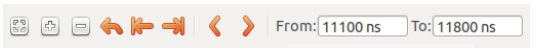
EXECUTION OF THE FIRST SW INSTRUCTION:

We first analyse the execution of the first `sw` instruction that writes the GPIO Enable Register with the value 0x0000FFFF.

- Assembly instruction: **`sw t3,0(t4)`**
- Machine instruction: **`0x01cea023`**

Set the time range to 11100ns-11800ns 

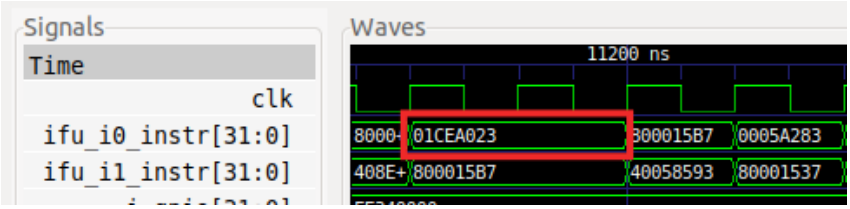
The store instruction (**`0x01cea023`**) is fetched around 11200ns, as shown in signal *ifu_i0_instr* (see Figure 1). The signal prefix indicates that it is part of the instruction fetch unit (*ifu*). It is in way 0 of the 2-way superscalar processor (*_i0*), and the signal is the instruction being fetched (*_instr*).

After several cycles (during which the instruction is decoded, executed… in the CPU), the write request is sent to the I/O system, as shown in Figure 1. Specifically, around 11500ns:

- The CPU sends the address to write (*wb_m2s_io_adr*=0x00001408) through the Wishbone bus. The address is provided to the multiplexer using signal *wb_io_adr_i*=0x00001408.

- Based on address 0x00001408 the multiplexer selects the GPIO slave (*match* = *0000010* and *wb_gpio_cyc_0*=1), connecting all its signals to the Wishbone bus that connects with the CPU. Specifically:
  - **wb_gpio_dat_o = wb_io_dat_i = 0x0000FFFF** (Value provided to the GPIO by the store instruction)
  - **wb_gpio_adr_o = wb_io_adr_i = 0x00001408** (Address provided to the GPIO, that corresponds to the enable register).

- Finally, 1 cycle after the multiplexer makes its selection, the Enable Register (*ext_padoe_o*) is updated with the value provided by the store: **ext_padoe_o=0x0000FFFF**.



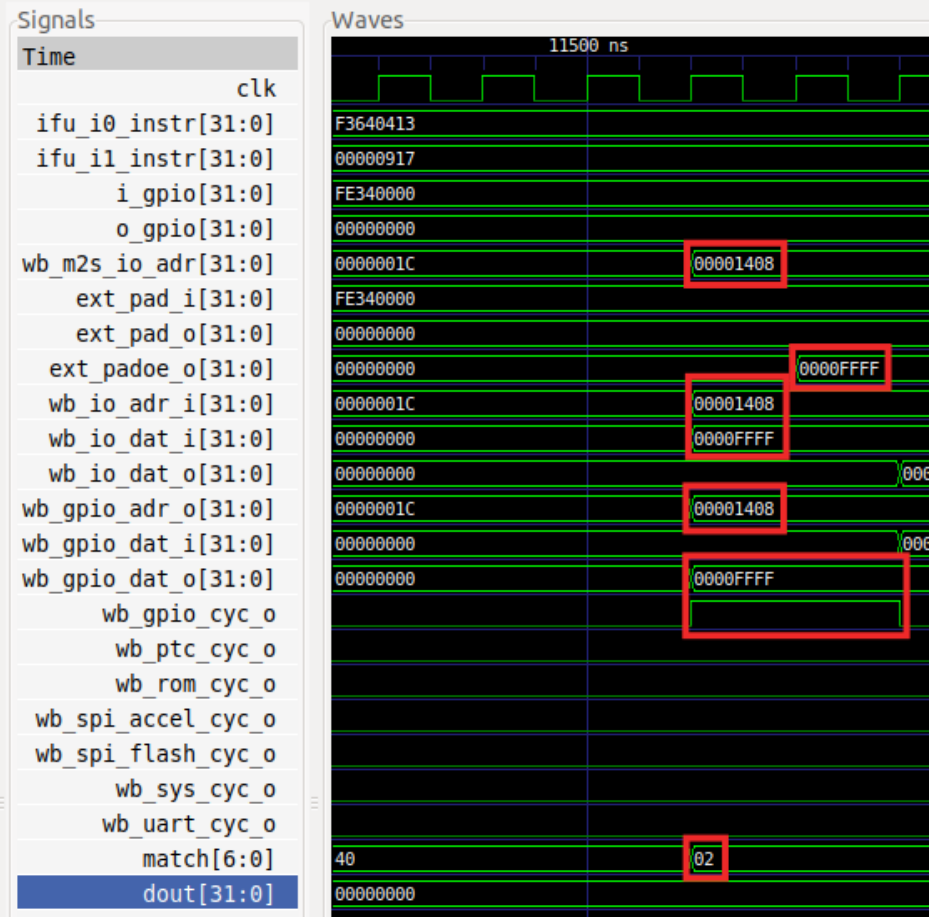


Figure 1. Simulation of the Enable Register write

EXECUTION OF THE LW INSTRUCTION:

We now analyse the execution of the `lw` instruction that reads the value of the Switches.

- Assembly instruction: **`lw t0,0(a1)`**
- Machine instruction: **`0x0005a283`**

Set the same time range as 11100ns-12000ns. The load instruction (**`0x0005a283`**) is fetched around 11200ns in *ifu_i0_instr* (see Figure 2).

After several cycles (during which the instruction is decoded and executed in the CPU), the read request is sent to the I/O system. Specifically,

- The value of the switches is provided into the GPIO module through signals *i_gpio* and *ext_pad_i* (you can review the code from Figure 2). You can verify in the figure that the value simulated for the switches in the testbench is 0xFE34, as this is the value contained in signals *i_gpio[31:16]* and *ext_pad_i[31:16]*.

- The CPU sends the address to write (*wb_m2s_io_adr*=0x80001400) through the Wishbone bus. The address is provided to the multiplexer using signal *wb_io_adr_i*=0x80001400.

- Based on address 0x00001400 the multiplexer selects the GPIO slave (*match* = *0000010* and *wb_gpio_cyc_0*=1), connecting all its signals to the Wishbone bus that connects with the CPU. In particular, in the simulation, you can see that:
  - **wb_io_dat_o = wb_gpio_dat_i = 0xFE340000** (value provided by the GPIO due to the load instruction).
  - **wb_gpio_adr_o = wb_io_adr_i = 0x00001400** (Address provided to the GPIO, that corresponds to the read register).

- Finally, note that, several cycles later, register t0 (signal *dout* in the simulation) is updated with the value read from the switches: **dout[31:16]=0xFE34**.

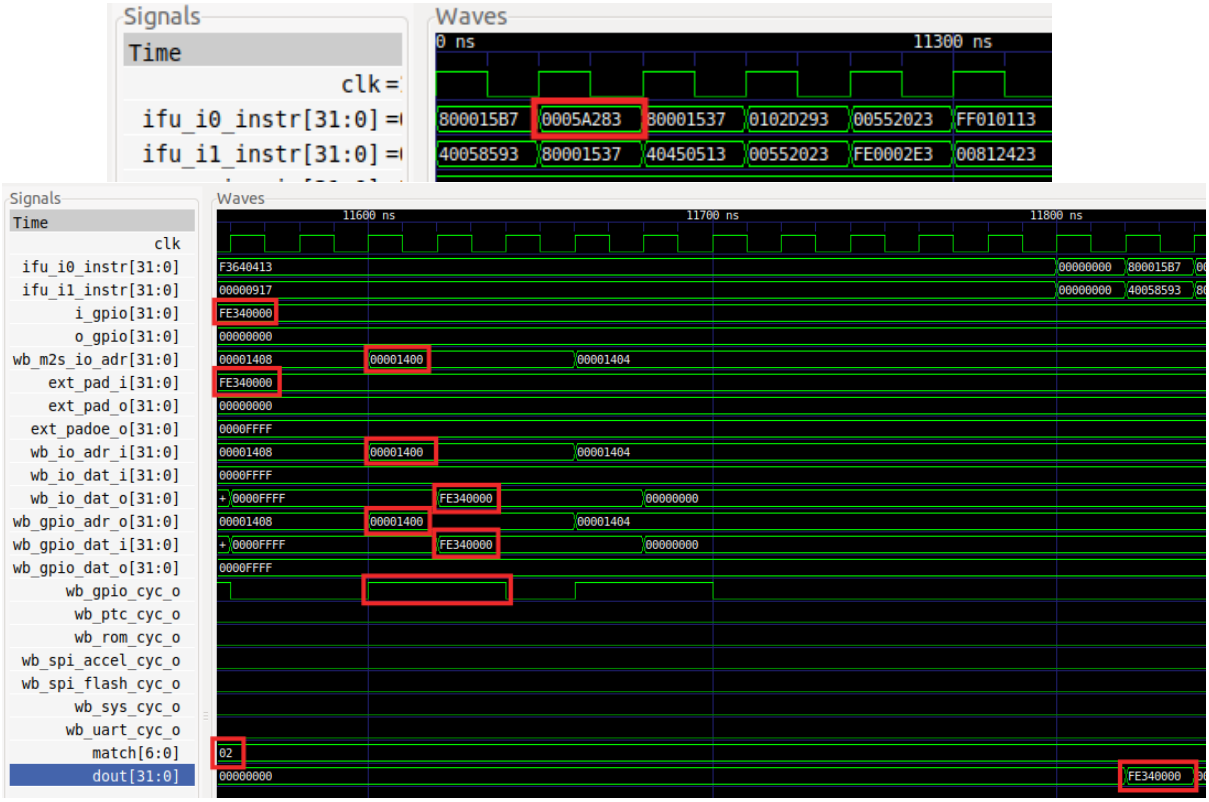


Figure 2. Simulation of the Switches reading

EXECUTION OF THE SECOND SW INSTRUCTION:

We finally analyse the execution of the second `sw` instruction that sets the LED values.

- Assembly instruction: **`sw t0,0(a0)`**
- Machine instruction: **`0x00552023`**

Set the time range to 11200ns-12300ns. The store instruction (**`0x00552023`**) is fetched in *ifu_i1_instr* around 11300ns (see Figure 3).

After several cycles (during which the instruction is decoded and executed in the CPU), the write request is sent to the I/O system. Analyse Figure 3 guided by the following steps:

- The CPU sends the address to write (*wb_m2s_io_adr*=0x80001404) through the Wishbone bus. The address is provided to the multiplexer using signal *wb_io_adr_i*=0x80001404.

- Based on address 0x00001404 the multiplexer selects the GPIO slave (*match* = *0000010* and *wb_gpio_cyc_0*=1), connecting all its signals to the Wishbone bus that connects with the CPU. Specifically:
  - **wb_gpio_dat_o = wb_io_dat_i = 0x0000FE34** (Value provided to the GPIO by the store instruction)
  - **wb_gpio_adr_o = wb_io_adr_i = 0x00001404** (Address provided to the GPIO, that corresponds to the enable register).

- Finally, 1 cycle after the multiplexer makes its selection, *ext_pad_o* is updated with the value provided by the store: **ext_padoe_o=0x0000FE34**. That value is provided to the LEDs through signal **o_gpio=0x0000FE34**.

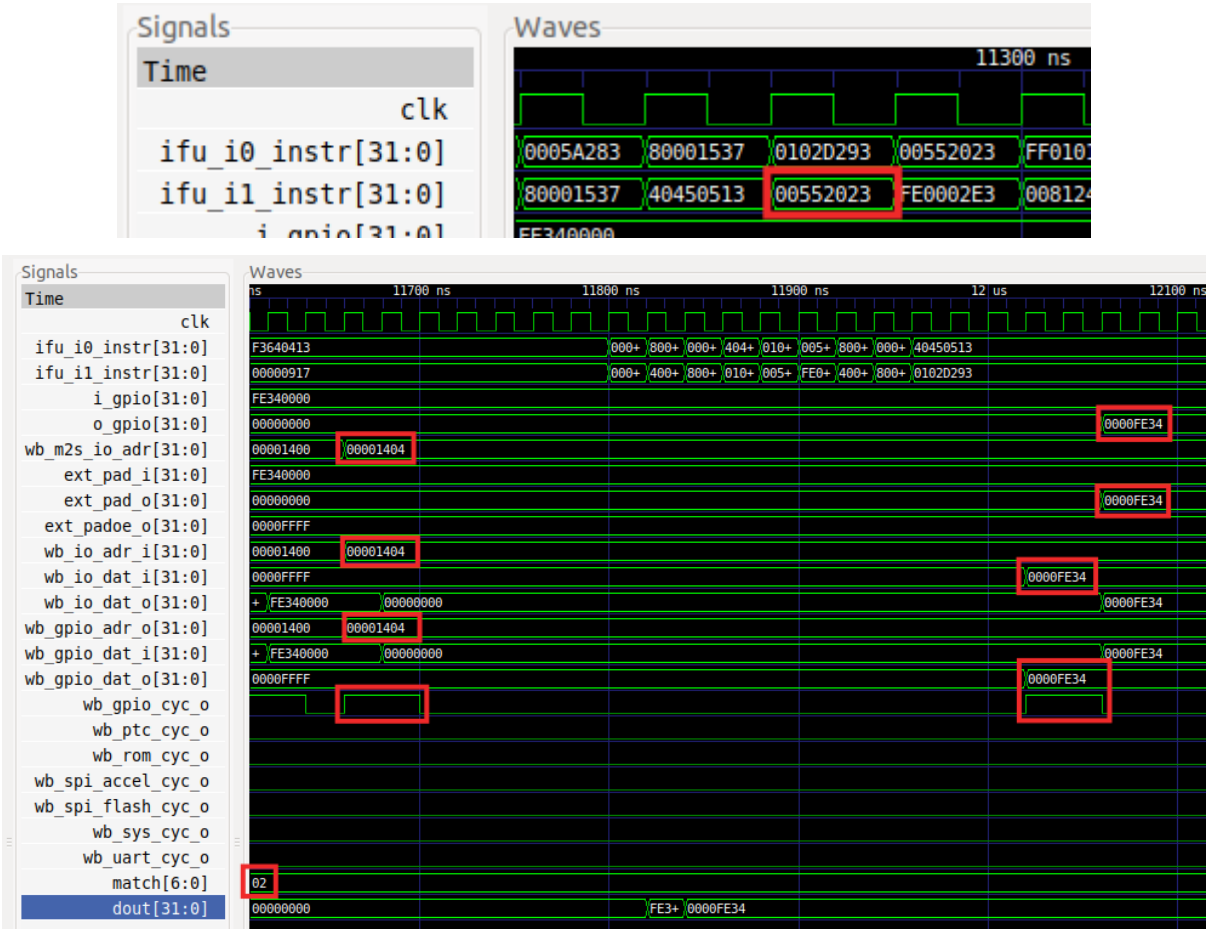


Figure 3. Simulation of the LEDs writing