

IMAGINATION UNIVERSITY PROGRAMME



Let us empower you to use our technologies in your teaching labs and student projects!
We have 29 years' experience of helping teachers around the world...

The four vital components in our teaching packages:

Tools: free to download software development tools. Full versions with no code size or time limits!

Hardware: low-cost, robust, and effective hardware from our partners

Materials: not in-house/commercial training. Genuine teaching materials written by academics who are respected experts in their field. With licensing that allows sharing with students, editing, translation and unrestricted academic/not-for-profit use

Effective support: through our forums, online video tutorials, and online/on-campus workshops

The majors & courses we focus on:

- Computer Science/Engineering ("CS"/"CE")
- Games Design/Engineering/Programming
- Electrical & Electronic Engineering ("EE")
- Automotive Engineering
- Computer Architecture
- System-on-Chip ("SoC") Design
- Graphics
- GPU Acceleration & Compute
- AI: Artificial Intelligence
- Autonomous Vehicles and In-Vehicle Systems



Introduction to Mobile Graphics

Scope:

The first course on Mobile Graphics, with Lectures and Labs. A full semester course.

Author:

Darren McKie, University of Hull, UK

Partners:

BeagleBoard.org

Audience:

3rd year BSc/MSc Gaming, EE and CS Students

Hardware:

Acer Chromebook, Android phones / tablets, BeagleBone Black/AI 64
OR: Software Emulator on a PC

Online Video Tutorials

One Day Workshop: materials & package and videos from April'22
London Workshop

Online self-study course in Chinese on XuetangX

Languages:

English, Chinese (simplified & traditional),
Japanese, Korean

Support:

IUP Forum: university.imgtec.com/forums

Request & Download:

university.imgtec.com/teaching-download

Tool-Chain: PowerVR SDK

| Week | Lecture Topic | Details |
|------|--|--|
| 1 | Introduction to mobile graphics technologies | Introduction to the different graphics APIs available and how they compare. |
| 1-2 | Basics of the PowerVR Framework, and simple Object Orientated Design | How the simple triangle graphics program has been written using the PowerVR SDK. How to separate the triangle code out of the main drawing function and into its own class. |
| 2-3 | Introduction to mobile graphics architectures | Comparison of mobile's dominant graphics hardware, an introduction to the concerns relating to power consumption and performance, and to understand the cross-platform/cross-compilation benefits of OpenGL ES. The PowerVR Graphics architecture case study will be outlined. |
| 3-4 | Introduction to graphics SDKs and forums | Learn about the main technologies used in mobile graphics SDKs up to OpenGL ES 3.2 and to learn how to use some of the SDK utilities and how to use forums for help. |
| 4-5 | Texturing | How texturing works, including the coordinate system and performance concerns. |
| 5 | Transformations | How transformations and lighting can be applied to vertices, including translations, rotations, and how to apply lighting. |
| 6-7 | OpenGL ES basics | Learn the basics of the OpenGL ES commands and Shader Language. |
| 7-8 | OpenGL ES lighting | Learn how to use different lighting models to illuminate objects in a scene. |
| 9 | Reflection and Refraction | Learn how cubemaps can be created and how they are used for calculating reflections and refractions. |
| 9-10 | Introduction to Vulkan | Introduction to Vulkan and a comparison with OpenGL ES. |

Overview of RVfpga Courses

The RVfpga: Understanding Computer Architecture course targets a soft-core RISC-V CPU – the SweRV EH1 - to an FPGA. It guides users in setting up the tools and ensuring the system is working. Through twenty well-documented and thorough labs, it enables students to understand the workings of the CPU, its interfaces to the outside world, and its core, pipeline, and memory system.

The follow-on course, RVfpga-SoC: An Introduction to SoC Design, enables users to gain hands-on experience building a System-on-Chip (SoC). RVfpga-SoC guides users through the interconnect options, adding peripherals, and then running an RTOS (real-time operating system) on the SoC. This course includes five labs including one that shows how to run Tensorflow Lite on the SoC.

Both courses use the RVfpga system, which is based on Chips Alliance's SweRVolf SoC that uses Western Digital's RISC-V SweRV EH1 core. SweRV EH1 is a fully-verified production-level processor core. SweRV EH1 is open-source and is already in silicon, including in Western Digital's SSD data storage and in Imagination Technologies' latest GPUs.

We are passionate about sharing real-world in-silicon solutions with students and other RISC-V users. Why use a "simplified education core" when you can use industrially proven designs? SweRV cores are at the centre of a vibrant expanding ecosystem with many useful open-source and commercial tools available, including simulators, models, integrated development environments (IDEs), virtual hardware, and pre-configured FPGA-ready SoC implementations.

Scope

The teaching materials fully illustrate the fundamentals of computer architecture, the inner workings of a RISC processor, and the process to get from a CPU to a System-on-Chip Design.

Authors

Dr. Sarah Harris, University of Nevada, Las Vegas (U.S.),
Dr. Daniel Chaver-Martínez, Universidad Complutense de Madrid (Spain), Zubair Kakakhel (AKZY Ltd; UK)

Audience

BSc Digital Design & Microarchitectures, Computer Organisation & Architecture, BSc/MSc Advanced Computer Architecture, MSc SoC design, MSc Design Verification, BSc/MSc Embedded Systems projects and MSc/PhD Processor Architecture

Languages

English, Chinese (simplified & traditional), Japanese, Korean, Russian, Spanish, Portuguese and Turkish

Software

- Xilinx Vivado 2019.2 WebPACK
- Microsoft's Visual Studio Code
- PlatformIO with Chips Alliance platform, which includes: RISC-V Tool-chain, OpenOCD, Verilator HDL Simulator, Western Digital's Whisper ISS (instruction set simulator)

Hardware

- Digilent Nexys A7 (100T) or Nexys 4 DDR FPGA Board

Hardware is recommended but not required:

- All labs can be completed in simulation, or using "ViDBo" the Virtual Development Board.

Open source RISC-V Core & SoC

- Core: Western Digital's SweRV EH1
- SoC: Chips Alliance's SweRVolf

Understanding Computer Architecture and Introduction to SoC Design

RVfpga (RISC-V FPGA) provides the foundation knowledge and hands-on experience that the next generation of programmers and engineers need to harness the potential of RISC-V. The course is suitable for undergraduate and master's classes, self-study, and industry training. It includes many resources for instructors who would like to teach RVfpga, including: how to set up the course, how to install hardware and software tools, lecture slides, lab instructions, examples and exercises with solutions, and supplementary materials. Instructors could use a subset of the materials in a single-semester course or run a two- to three-semester course using all of the materials.

Additional features & support:

- A Getting Started Guide and twenty labs with detailed instructions, examples, short questions and practical exercises with solutions, giving teachers flexibility to choose between a practical and an exam-based structure for the course.
- Provided in both PDF and .pptx/.docx formats enabling customisation by teachers to suit their own needs.
- Available in nine languages: English, Simplified Chinese, Traditional Chinese, Japanese, Korean, Spanish, Turkish, Russian, and Portuguese.
- Direct support and up-to-date news on Imagination University Programme Forum: university.imgtec.com/forums

RVfpga: Sponsors & Supporters

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Semesters 1&2: RVfpga: Understanding Computer Architecture

| Lecture Topic | Details |
|---------------|--|
| Lab 0 | RVfpga Labs Overview |
| Lab 1 | C Programming |
| Lab 2 | RISC-V Assembly Language |
| Lab 3 | Function Calls |
| Lab 4 | Image Processing: Projects with C & Assembly |
| Lab 5 | Creating a Vivado Project |
| Lab 6 | Introduction to I/O |
| Lab 7 | 7-Segment Displays |
| Lab 8 | Timers |
| Lab 9 | Interrupt-Driven I/O |
| Lab 10 | Serial Buses |
| Lab 11 | SweRV EH1 Configuration and Organization. Performance Monitoring |
| Lab 12 | Arithmetic/Logical Instructions: the add instruction |
| Lab 13 | Memory Instructions: the lw and sw instructions |
| Lab 14 | Structural Hazards |
| Lab 15 | Data Hazards |
| Lab 16 | Control Hazards. Branch Instructions: the beq Instruction. The Branch Predictor. |
| Lab 17 | Superscalar Execution |
| Lab 18 | Adding New Features (Instructions, Hardware Counters) to the Core |
| Lab 19 | Memory Hierarchy. The Instruction Cache. |
| Lab 20 | ICCM and DCCM |

Semester 3: RVfpga-SoC: Introduction to SoC Design

| Lecture Topic | Details |
|---------------|---|
| Lab 1 | Introduction to RVfpga-SoC |
| Lab 2 | Running Software on the RVfpga SoC |
| Lab 3 | Introduction to SweRVolf and FuseSoC |
| Lab 4 | Building and Running Zephyr on the SweRVolf |
| Lab 5 | Running Tensorflow Lite on SweRVolf |

Guide to RISC-V

RISC-V is big news in the semiconductor industry. What's behind the buzz? We've teamed up with Digi-Key to create a technology guide focused on RISC-V. Short, easy to understand, and hands-on. Written by Richard J. Sikora, it draws on his 35 years' experience in embedded systems development!

Contents

- RISC-V: its history and unique features
- Licencing
- Where the technology is going...
- Early examples of implementations
- Hands-on with three implementations:

Real-World Examples

- (1) MPU microprocessor running Linux using the Kendryte CPU on the Seeed Technologies Maix BiT board.

- (2) MCU microcontroller using the SiFive SoC on the SparkFun RED-V "Red Board".

- (3) And a "soft core" – implementing Western Digital's "SweRV" EH1 core on an FPGA from Xilinx – the platform for our "Rvfpga" Teaching Materials.

Direct Download

university.imgtec.com/resources/download/guidetoriscv

Fun with Beagle – Exploring the GPU & Running OpenCL

The BeagleBone® Black is a favourite development platform for millions of users: Students, Hobbyists, and Developers. It has become a preferred Single Board Linux Computer for industrial developers. The TI "Sitara™" system-on-chip at the heart of Beagle contains an Imagination SGX530 GPU. Until now, this was just a block on the system diagram and a "black box" to most Beagle users. In recognition of Beagle's popularity, we are lifting the lid on its GPU...

Dr. Iain Hunter was at TI when the Sitara SoCs first appeared, and since then he has become a leading independent developer on this platform. Few people know Beagle so well!

Graphics

Materials from "Introduction to Mobile Graphics, 2020 Edition" run on Beagle, and this guide reprises some basic examples.

Running Open CL

Dr. Hunter takes you through this interesting and quite complex part of the BeagleBone Black system. He shows you how to implement Open CL on the GPU and run an application.

- The package includes the Open CL driver along with a practical explanation about getting it running and how to use it
- The example demonstrates Audio Sample Rate Conversion, running on the GPU – a first for the Beagle Board!

Online Video Tutorials

- Preparation
- Boot BeagleBone Black
- Configure SDK
- Compile SDK
- Build BeagleBone Black OpenCL Examples
- Run BeagleBone Black OpenCL
- Build OpenCL audio
- Run ALSA OpenCL

Edge AI – Principles and Practices

Scope

The full course is based on the development of 4 module, 9 units and 11 labs (L0-L10), which will cover the fundamental algorithms and typical applications in Edge AI, following a case-study format and fitting a typical semester course.

Authors

Prof. Luis Pinuel Moreno, Prof. Francisco D. Igual - Universidad Complutense de Madrid (Spain), Prof. Sandra Catalán, Rafael Rodriguez

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Platform

BeagleBone AI 64 board running Imagination's Neural Compute Software Development Kit (NC-SDK-AC)

Audience

3rd year BSc EE and CS Students

Languages

English, Chinese (simplified) to follow

| Week | Lecture Topic | Details |
|---|---|---|
| Module 1. Introduction to Edge AI | 1. Introduction and Getting Started | Introduction to Edge AI and the experimental platform |
| | | Lab 0: Getting started with the Pumpkin board |
| | 2. Data acquisition and processing on the Edge | Image processing fundamentals |
| | | Lab 1: Image acquisition and processing with OpenCV |
| | 3. Introduction to Machine Learning on the Edge | Introduction to Machine Learning, the IMG Neural Compute SDK and the IMGDNN library |
| | | Lab 2: First steps with the NCSDK |
| | | Lab 3: My first Neural Network on the Pumpkin board |
| Module 2. Image vision | 4. Image classification | Image classification on edge device |
| | | Lab 5: Image classifier example on the Pumpkin board |
| | 5. Image segmentation | Image segmentation on Edge devices |
| | | Lab 6: Semantic image segmentation on the Pumpkin board |
| | 6. Object detection | Object detection on Edge devices |
| | | Lab 7: SSD person detection on the Pumpkin board |
| Module 3. Speech and natural language processing | 7. Automatic Speech Recognition (ASR) | Automatic Speech Recognition for Edge Devices |
| | | Lab 8: Voice control of the Pumpkin board |
| | 8. Natural Language Processing (NLP) | NLP Fundamentals |
| | | Lab 9: Automatic question answering on the Pumpkin board |
| Module 4. Advanced topics | 9: Advanced NCSDK and OpenCL usage. | Advanced NCSDK and OpenCL usage. |
| | | Lab 10: OpenCL-based pre- and post-processing |

IUP Website

The focal point to access our services is the IUP website: teaching materials, video tutorials, forums, suggested hardware, recommended textbooks, pictures, news, and workshop + event listings.



Joining the IUP

Visit Imagination University Programme website:
university.imgtec.com

Click Register on the menu bar

Fill in the registration form. Please make sure you fill in the items with green star

After submission, you will receive an email to set up your password

Requesting teaching materials

Request the materials you want

Tell us what you plan to do

We will assess and respond to your request within 3 working days

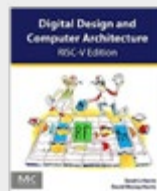
Once approved, you will receive an email with the download link. Be quick - this link is only valid for 3 days

Useful Textbooks



Computer Graphics: Principles and Practice (3rd Edition)

John F. Hughes & Andries van Dam
Available in Chinese and English



Digital Design & Computer Architecture (RISC-V Edition)

Sarah Harris & David Harris - Sept'21
Available in Chinese and English



Deep Learning (Adaptive Computation and Machine Learning series)

Ian Goodfellow, Yoshua Bengio, Aaron Courville
Available in Chinese and English

Hardware Tools



Digilent Nexys A7-100T

Based on Xilinx Artix®-7 FPGA. The -100T can hold the Western Digital SweRV software. 7-segment digital displays & rich I/O make it a great fit for computer architecture labs. The older Nexys 4 DDR is also suitable.



Pumpkin i300 EVK

Based on the MediaTek i300B SoC, ARM Quad-Core A35 1.3GHz processor, PowerVR 8XE GPU which supports OpenGL, OpenGL ES and OpenCL. Together with the Neural Compute SDK Academic version, it could become an ideal platform for you to run Edge AI applications.



BeagleBone® Black

The BeagleBone Black from beagleboard.org is based on the TI AM335x Arm Cortex-A8 processor 512MB DDR3 RAM, PowerVR SGX530 GPU with 3D graphics accelerator, microSD card, HDMI, Ethernet, USB 2.0, 2x PRU 32-bit microcontrollers